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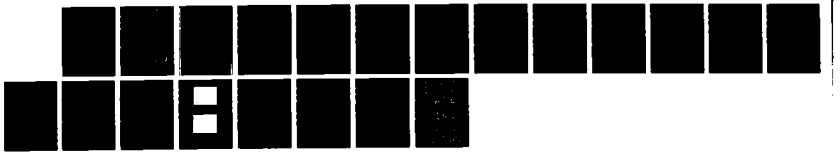

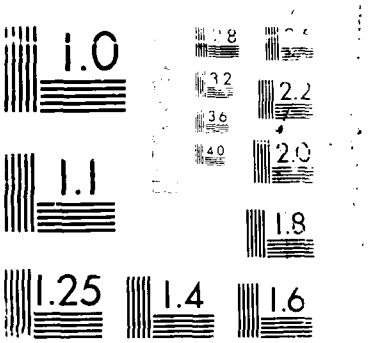
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Mesa expitaxial and planar implanted InP power MISFET's have been fabricated. At 9.7 GHz CW mesa devices demonstrated 4.5W ouput with 4 dB gain at 46 percent power-added efficiency with a power density of 4.5W/mm, over three times the highest value ever reported for GaAs FET's. Power output is stable with 2 percent over 167h continuous operation. Planar implanted devices exhibited 3.5W output with 5.4 dB gain, 40 percent power-added efficiency and 3.5W/mm power density at 9.7 GHz.

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features with respect to high mechanical stability, electromechanical efficiency, and positioning accuracy, especially at low temperatures, is discussed. Another aspect is the influence of cool-down on the electrodynamical behavior of the system.

392 A Survey of Cryogenic Apparatus Available to Support Electronic and Electro-Optic Studies over the Temperature Range of 4.2-300 Kelvin: *R. G. Hansen*, R. G. Hansen & Associates, Santa Barbara, CA 93101

With the recent emphasis on the characterization of electronic and electro-optical devices and their temperature dependent characteristics at cryogenic temperatures, we believe that a survey of available cryogenic apparatus is a valuable reference to the researcher. A comprehensive survey and the advantages of various cryogenic techniques are discussed A survey of state-of-the-art high speed, low noise measurement apparatus is reviewed.

393 The Use of Automated Laboratory Test Equipment for the Characterization of Electronics at Cryogenic Temperatures: *C. N. Magoun*, R. G. Hansen & Associates, Santa Barbara, CA 93101

Recent developments in the integration of PC computers and automated temperature controllers with commercially available laboratory cryogenic systems for the characterization of electronics and electro-optic devices for space are discussed. With the recent emphasis on the reliability of electronic systems and components in a "space environment," considerable emphasis is placed on the thermal cycling of electro-optic and electronic equipment. With the current availability of dedicated computers with programmable temperature indicators and controllers, a vast new capability is available to the researcher. A recent experience in the integration of this equipment is discussed.

394 The Direct Chip Probe/Test System (DCP/T): *J. G. Doherty*, Teledyne TAC, Woburn, MA 01801

Developed under U.S. Army Manufacturing Methods and Technology Project No. 1060 entitled "Electrical Test and Screening of Semiconductor Chips," the DCP/T is a fully automatic handling system that aligns and tests semiconductor devices from −70°C up to 200°C. The DCP/T eliminates the present method of "the mount-bond-test approach" where the device must be mounted into a carrier, wire-bonded to metallization on the carrier, and tested at temperature via carrier pin-out interconnections.

DIELECTRICS AND INSULATION/ELECTRONICS

Dielectric Films on Compound Semiconductors

395 MMIC Development at NASA Lewis Research Center: *R. F. Leonard*, NASA Lewis Research Center, Solid State Technology Branch, Cleveland, OH 44135

NASA's Lewis Research Center is actively involved in the development of monolithic microwave and millimeter wave integrated circuits. The approach of the program is to support basic research under grant or in-house, while MMIC development is done under contract, thereby facilitating the transfer of technology to users. Primary thrusts of the program have been the extension of technology to higher frequencies (60 GHz), degrees of complexity, and performance (power, efficiency, noise figure, etc.) by utilizing new circuit designs, processes, and materials.

396 Effects of Photochemical Treatments on Surface Properties of GaAs: *T. Sawada, H. Hasegawa,* H. Yano*, and *H. Ohno*, Dept. of Electrical Engineering, Faculty of Engineering, Hokkaido University, Sapporo 060, Japan

Effects of photochemical oxidation in water and of photochemical treatment in NH_3 on surface properties of GaAs are critically investigated by transverse transport, MIS C-V, photoluminescence and XPS measurements. Photochemical oxidation resulted in enhanced pinning with enhanced PL intensity rather than in "unpinning" as previously reported. Treatment in NH_3 under ArF excimer laser reduced pinning with reduced PL intensity. The result is explained by a rigorous computer simulation showing that higher N_{ss} can give enhanced photoluminescence under certain conditions.

397 Silicon Nitride Films Deposited by ECR Plasma CVD for Application to GaAs Ion-Implantation Process: *D. Inoue,* M. Sawada*, and *Y. Harada*, Research Center, Sanyo Electric Co., Ltd., 1-18-13 Hashiridani, Hirakata, Osaka 573, Japan

The development of a rapid thermal annealing technique for implanted GaAs wafers covered with SiN films is very important for the fabrication of GaAs IC's. The SiN films used in this process play the role of (i) an encapsulation for the annealing, and (ii) through-implantations and encapsulation. Films with properties which satisfy item (i) above, have been newly developed by ECR plasma CVD.

398 Power MISFET's on InP: *L. Messick,* D. A. Collins, R. Nguyen, A. R. Clawson*, and *G. E. McWilliams*, Naval Ocean Systems Center, Electronic Material Sciences Division, San Diego, CA 09152-5000

Mesa epitaxial and planar implanted InP power MISFET's have been fabricated. At 9.7 GHz CW mesa devices demonstrated 4.5W output with 4 dB gain at 46% power-added efficiency with a power density of 4.5 W/mm, over three times the highest value ever reported for GaAs FET's. Power output is stable within 2% over 167h continuous operation. Planar implanted devices exhibited 3.5W output with 5.4 dB gain, 40% power-added efficiency and 3.5 W/mm power density at 9.7 GHz.

399 Plasma-Deposited Germanium Nitride on Indium Phosphide: *G. A. Johnson,* V. J. Kapoor*, and *P. G. Young*, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221-0030

Germanium nitride (Ge_3N_4) films were deposited on indium phosphide compound semiconductor substrates using plasma-enhanced chemical vapor deposition with 5% germane in argon, nitrogen, and nitrogen/ammonia mixtures as reactant gases. The refractive index of the films was determined by ellipsometry to be in the range of 1.9-2.2. Depth profiles obtained using Auger electron spectroscopy were used to compare the composition of films deposited using GeH_4/N_2 and $GeH_4/NH_3/N_2$ gas mixtures. In addition, infrared spectroscopy was used to compare the hydrogen content of the films. MIS capacitors were used to determine the electrical properties of the films. In order to demonstrate the feasibility of germanium nitride as a gate insulator, InP MISFET's were fabricated and exhibited transistor action.

400 Ultrashort Gaps Between Schottky Barriers Formed by Anodization: *P. B. Kose** and *D. S. Katzer*, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221

Schottky barrier charge-coupled devices with overlapping metal electrodes on semi-insulating gallium arsenide have been demonstrated. The thin dielectric isolation (500Å) between the electrodes was formed by anodic oxidation in an ethylene glycol based electrolyte. The overlapping gate structure imitates that of the close-packed overlapping polysilicon gate CCD's formed on silicon. The device active channels were formed by ion implantation and rapid thermal annealing with silicon nitride used as a cap. The anodic oxidation was performed after all high temperature processing steps, including ohmic contact alloying, were complete. This preserves good electrical properties of the anodic oxides and has yielded working CCD's operating with 5V clock amplitudes.

401 Tantalum as Mask in the Fabrication of CCD's on GaAs: *P. B. Kosel* and *E. Miller,** Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221

Two masking requirements exist in the production of CCD's on gallium arsenide: (i) to mask the first level aluminum electrodes against anodic oxide growth in regions where intermetal contacts are to be made, and (ii) to protect the silicon nitride cap against electrical breakdown at high voltages that arise during the anodic growth process. In both cases, tantalum metal films formed by sputtering have been used as the anodization protect masking layer. Tantalum films have been found to be particularly well suited to this application because (i) it is an anodizable metal, and (ii) it and its anodic oxide can be readily etched in a CF_4 plasma. Hence, it provides a useful medium for differential masking of aluminum and gallium oxides that are not etched by the CF_4 plasma. Details of the process and device characteristics are presented.

402 Effects of Plasma Deposition Frequency on Material Properties of SiN Thin Films: *J. J. Pouch,** NASA Lewis Research Center, Cleveland, OH 44135, *D. M. Pantic*, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221, *S. A. Alterovitz, K. Miyoshi, J. D. Warner, J. E. Dickman*, and *W. D. Williams*, NASA Lewis Research Center, Cleveland, OH 44135

Studies were made to determine the changes in the material properties resulting from a variation of the plasma discharge frequency for plasma deposited silicon nitride. Silicon nitride was plasma deposited on substrates of silicon, gallium arsenide, and indium phosphide. The composition of the thin films and the interfaces between the dielectric films and the semiconductor substrates were examined by optical and surface techniques.

403 Rapid Thermal Annealing of Ion-Implanted Indium Phosphide: *M. D. Biedenbender,* V. J. Kapoor*, and *D. Xu*, Dept. of Electrical and Computer Engineering, University of Cincinnati, Cincinnati, OH 45221-0030, *W. D. Williams*, NASA-Lewis Research Center, Cleveland, OH 44135

Rapid thermal annealing of ion-implanted indium phosphide has been investigated. The implantation species investigated was silicon, and the encapsulant used was silicon nitride. Substrates were rapid thermal annealed for various times in either nitrogen or hydrogen ambients. Encapsulant-substrate interactions were studied using Auger electron spectroscopy depth profiling and a sequence of high resolution x-ray photoelectron spectroscopy measurements. Atomic concentration profiles were investigated using secondary ion mass spectrometry. Electrical properties of implanted regions and test structures were analyzed by fabricating MISFET's. The sheet resistivity, IV characteristics, and other transistor properties were observed for several device geometries.

404 Interface Properties of InP-Dielectric Systems: *P. Viktorovitch*, Laboratoire D'Electronique — UA CNRS 848, Ecole Centrale de Lyon — BP 163, 69131 Ecully Cedex, France

The development of appropriate passivation schemes for III-V compound semiconductors is of considerable interest for application to high speed, high power, and electro-optic devices and integrated circuits. In this paper, special attention is given to InP in connection with insulated gate technology for MISFET's applications. A review of the techniques of fabrication of dielectric-InP systems is presented along with the main techniques of characterization developed in our group to analyze their electronical and

To be published in the "Proceedings of the 2nd Symposium on Dielectric Films on Compound Semiconductors," held at the 172nd Meeting of the Electrochemical Society Honolulu, Hawaii, October 18-23, 1987.

POWER MISFETs ON InP

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A. R. Clawson, G. E. McWilliams and T. Vu
Electronic Material Sciences Division (Code 56)
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San Diego, CA 92152-5000

ABSTRACT

Mesa-type epitaxial and planar fully ion-implanted indium phosphide (InP) n-channel depletion-mode power MISFETs have been fabricated on Fe-doped semi-insulating substrates using SiO_2 as the gate insulator. At 9.7 GHz CW mesa-type epitaxial devices demonstrated 4.5 W output with 4 dB gain at 46% power-added efficiency with a power density of 4.5 W per mm of gate width, over three times the highest value ever reported for GaAs FETs. Power output is stable to within 2% over 167 hours of continuous operation. Also at 9.7 GHz CW the planar fully ion-implanted devices exhibited a power density of 2.9 W per mm of gate width, about twice the highest GaAs FET value.

INTRODUCTION

Recent results on InP MISFETs (1-3) have demonstrated that these devices are very attractive for high frequency power applications. Table I lists a number of advantages of these structures as compared to GaAs FETs. The peak electron drift velocity in InP is approximately 2.2×10^7 cm/sec. as compared to a 1.7×10^7 cm/sec. in GaAs (3). The thermal conductivity of InP is 0.7 W/cm-°C compared to 0.5 for GaAs (3). The breakdown field in InP is 530 kV/cm (4) compared to 390 in GaAs (5) for $\alpha_n = 10^4 cm^{-1}$. The gate insulator in a MISFET structure constitutes a physical barrier against gate metal diffusion into the channel, an aspect which could prove beneficial in relation to device lifetime and reliability. The gate insulator also makes possible large positive gate voltages, typically greater than 20 V without gate breakdown.

Another advantage of the insulated gate is that it makes possible carrier accumulation in the channel. From capacitance versus voltage measurements on MIS structures it can be seen that for zero gate voltage the InP surface is accumulated at the interface with the SiO_2 gate insulator. This charge accumulation provides the channel

with a carrier density greater than that provided by the doping alone and therefore may be beneficial with regard to mobility. A comparison between ungated channel saturation current before and after deposition of the gate insulator shows roughly a 30% current increase upon insulator deposition. This is presumably attributable to charge carrier accumulation. Of course the application of positive gate voltage will increase this accumulation effect.

The gate leakage current is much lower for an insulated gate device than for such structures as MESFETs, JFETs and heterojunction gate FETs. This gives the InP MISFET an important advantage over devices not having truly insulated gates, including InP MESFETs (6) which exhibit relatively high gate leakage and low source-drain breakdown voltage apparently as a result.

Together the advantages discussed thus far suggest that InP MISFETs should exhibit higher power output per unit gate width (power density) (1-3) than GaAs FETs, a prediction which has been experimentally verified. InP MISFETs (1-3) have demonstrated over three times the highest power density ever reported for GaAs FETs and because of their higher power densities these structures also promise much higher absolute power outputs than have been achieved with GaAs as soon as large enough devices are fabricated. While impressive results are being achieved with large gate width GaAs power MESFETs their low input impedance, which decreases with increasing gate width, leads to difficulties with their utilization in microwave systems (3) and limits the power achievable with such devices. This situation might be greatly improved by the use of a different material or device such as the InP MISFET for instance with higher power density and therefore higher input impedance for a given power output (3).

Table II lists disadvantages of InP power MISFETs as compared to GaAs FETs as well as features not yet known to favor one material or device over the other. InP has a slightly lower bandgap (1.3 eV as compared to 1.4 eV for GaAs at 300 K) is somewhat less mechanically durable and has a lower dissociation temperature than GaAs. Under strictly dc conditions these devices exhibit drain current drift due to charging or discharging of states residing in the neighborhood of the semiconductor/gate-insulator interface. However, when epitaxial InP MISFETs are used as high-frequency amplifiers the drift in power output is

extremely slight. Apparently the presence of an rf signal has a stabilizing effect on the interface states.

In the following section we shall review results from this laboratory concerning InP power MISFET structure, fabrication and performance.

DEVICE PROCESSING

We fabricated two kinds of devices, mesa-type structures fabricated on epitaxial InP layers and planar fully ion-implanted structures. Figure 1 illustrates a schematic cross section of an epitaxial device, an n-channel depletion-mode structure fabricated on an n-type epilayer with an initial thickness of approximately 0.7 μm and a doping density between 5×10^{16} and 2×10^{17} cm^{-3}. Following mesa definition, alloyed AuGe contact formation and evaporated Au contact pad definition the channels were chemically recessed with a 10% solution of HIO_3 in water to approximately 0.3 μm; the deep channel recess being important (3) for high-voltage high-power device operation.

Next the SiO_2 gate insulator was deposited to a thickness of about 1000 angstroms using remote-plasma-assisted CVD (7) at a temperature of approximately 300 °C using a gas mixture of SiH_4, O_2 and as a carrier gas N_2. Al gates with a thickness of 0.5 μm were then defined by evaporation and liftoff and finally bonding windows were opened in the SiO_2 layer. The source to drain spacing is approximately 4.5 μm and the gate length around 1.4 μm.

Figure 2 shows a cross-sectional representation of a typical ion-implanted device, an n-channel depletion-mode structure fabricated by implanting directly into a substrate of Fe-doped semi-insulating InP having a resistivity of $\geq 10^7$ ohm-cm. Contact regions selectively receive a multiple energy n^+ implant of Si ions using energies ranging from 40 to 360 keV and doses in the range 3×10^{13} cm^{-2} to 6×10^{14} cm^{-2}. The implant schedule is intended to produce a high-density relatively flat carrier profile from close to the surface to a depth great enough to provide a thorough contact to the implanted channel. High carrier density near the surface may be important for good ohmic contact formation. The precise schedule used is listed in figure 3 which illustrates the implanted impurity density versus depth (assuming Gaussian distributions with their first two moments predicted using Linhard, Scharff, Schiot (LSS) theory) resulting from each

individual energy implant as well as the total predicted density. Also shown in this figure are the results of an electrochemical carrier density profile measurement performed with a Polaron profiler on a semi-insulating Fe-doped InP control wafer which had been implanted with the specified schedule and then activated.

The channel region selectively receives a multiple energy n-type implant of Si which overlaps the n^+ contact implanted regions for electrical continuity. Channel implant energies range from 60 to 360 keV with doses from 1×10^{12} to 1.5×10^{13} cm^{-2}. In this case the schedule is intended to produce a carrier density in the low 10^{17} cm^{-3} range with as flat as possible a carrier profile from fairly close to the surface to a depth as great as possible with the maximum implantation energy available to us at the time (360 keV) falling off as abruptly as possible beyond such depth. Carrier density very near the surface is not critical in the channel region since, under the gate, approximately the first 0.3 μm of material is removed in the channel recessing fabrication step. A typical channel implant schedule, the corresponding predicted Si densities versus depth and measured resulting carrier density in an activated control wafer versus depth are shown in figure 4. After implantation the wafers are capped with approximately 2000 angstroms of SiO_2 and then annealed in forming gas at 725 °C for 60 seconds to electrically activate the implant. This activation recipe produced activations of ≈80% and mobilities ≈2000 $cm^2 V^{-1} sec^{-1}$ in Fe-doped InP test wafers which had received 50 keV Si implant doses of 5×10^{12} cm^{-2}.

Figure 5 illustrates one of the device geometries we used for the mesa-type expitaxial devices. For the sake of simplicity and clarity only the ohmic contact and gate metallization regions are shown. The areas marked "D" are isolated drain regions which must be individually wire bonded. The eight individual gate fingers are each 125 μm wide resulting in a total device gate width of 1 mm. Three other similar geometries with from three to five drain regions and from 750 μm to 1 mm total gate widths were also used. The geometries of the implanted devices were basically the same as those of the epitaxial structures.

RESULTS

Figure 6 shows an oscilloscope photograph of the drain characteristics of a representative 1 mm wide epitaxial device with a saturation current of approximately 660 mA per mm of gate width for a gate to source voltage of zero volts. The gate voltage is applied in 80 microsecond pulses. Figure 7 shows the drain characteristics of a typical implanted device.

Table III compares 8-10 GHz CW performance data for implanted and epitaxial InP MISFETs and the best ever reported GaAs FETs (8). The highest power per unit gate width at 4 dB gain for the epitaxial InP devices is 4.5 W/mm, over three times the highest value ever reported for a GaAs FET. The implanted InP MISFETs yielded about twice the best GaAs power density.

As was pointed out for epitaxial devices by Armand, et al. (3), the high power densities of both the InP structures are largely attributable to their high drain bias current per unit gate width, in this case around 330 mA/mm as compared to 127 mA/mm for GaAs (8). This high current per unit gate width arises from the high peak electron drift velocity in InP, the high product of channel thickness and doping density in these devices and from charge carrier accumulation in the channel.

The relatively inferior performance of implanted devices compared to epitaxial devices might be due, at least in part, to the transition between the semi-insulating substrate and the channel being inherently less abrupt in implanted structures as compared to epitaxial ones. Because of this at least part of the implanted channel has a lower than ideal doping density. Another partial cause might be the presence of Fe in device channels formed by direct implantation into the Fe-doped substrate. Possibly just a schedule including a deeper, higher-energy implant might effect an improvement by making possible a deeper channel recess. An advantage of implanted devices, however, is the greater ease, economy and reproducibility with which devices not requiring an epitaxial growth process can be fabricated and monolithically integrated with other devices.

Figure 8 illustrates at 9.7 GHz CW, for the same epitaxial InP MISFET as referred to in Table III, the dependence of power output, power-added efficiency and power gain on drain bias voltage and rf power input.

Optimum values of gate bias varied widely between devices while its effect on device performance was relatively small.

Figure 9 illustrates at the same frequency for a different device the variation of power output as a function of rf power input at a fixed drain bias voltage of 7.5 V; the power gain being 6.8 dB at 20.5 dBm power input. This value of power gain is typical of these devices at this rf power input and drain bias level.

Figure 9 also illustrates that the drain bias current for fixed gate and drain bias voltages is a decreasing function of rf power input (1,3). This effect appears to be due to the influence of the rf voltage applied to the MIS gate on the charge status of states residing in the neighborhood of the semiconductor/gate-insulator interface giving rise to an average channel depletion depth which decreases with increasing rf input power. Consequently when these devices are operated at high drain bias voltage with no average current limit on the bias supply a large reduction in the rf power input will increase the drain bias current as well as reduce the amount of dc power converted to rf. The device will then have more dc power to dissipate and thermal breakdown will result. For this reason safe operation at high drain bias voltage requires either that the rf input be maintained at a high level (1,3) or that the average drain current be limited. This effect, however, would present no problem for certain applications, for instance applications which don't necessarily require dc power to the device while the rf input is shut off, for example certain radar applications which only require pulses of constant rf power.

Figure 10 illustrates the time dependence of the power output and drain bias current of a representative epitaxial device with its dc drain bias voltage and its rf power input held constant, elapsed time equaling zero when these are first applied. For this device the power output was stable to within 2% over 167 hours of continuous operation despite a 10% drain bias current downward drift.

CONCLUSION

Table IV summarizes the best InP power MISFET results, which are for the epitaxial devices. Power output at 9.7 GHz CW with 4 dB gain is 4.5 W. The power density is 4.5 W/mm, over three times as much as ever reported for a GaAs FET. Maximum power-added efficiency observed is 50% and the power output is stable to within 2% over approximately one week of continuous operation, which is the longest we've looked at these devices so far.

In conclusion, InP power MISFETs promise to substantially advance high frequency power amplification beyond the capabilities of GaAs FETs.

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The authors thank N. T. Linh, Picogiga, Inc.; M. Armand, Thomson-CSF; J. Chevrier, Thomsom Semiconductors; H. M. Macksey, Texas Instruments and D. Rubin and A. K. Nedoluha, Naval Ocean Systems Center for numerous productive discussions.

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InP POWER MISFET ADVANTAGES OVER GaAs

HIGHER ELECTRON PEAK VELOCITY

HIGHER THERMAL CONDUCTIVITY

HIGHER BREAKDOWN FIELD

GATE-INSULATOR PREVENTS GATE METAL-DIFFUSION INTO CHANNEL

LARGE POSITIVE FIELD APPLICABLE TO INSULATED GATE

ACCUMULATION IN CHANNEL: (INCREASED CARRIER DENSITY WITHOUT INCREASED DOPING DENSITY)

LOWER GATE LEAKAGE CURRENT

HIGHER POWER PER UNIT GATE WIDTH (POWER DENSITY)

POTENTIALLY HIGHER POWER

HIGHER INPUT IMPEDANCE

Table I. Advantages of InP power MISFETs over GaAs.

InP POWER MISFET DISADVANTAGES COMPARED TO GaAs

LOWER BANDGAP

LOWER HARDNESS

LOWER DISASSOCIATION TEMPERATURE

CURRENT INSTABILITY (DRIFT)

UNDECIDED FEATURES

ELECTRON VELOCITY OVERSHOOT

NOISE

Table II. InP disadvantages and undecided features.

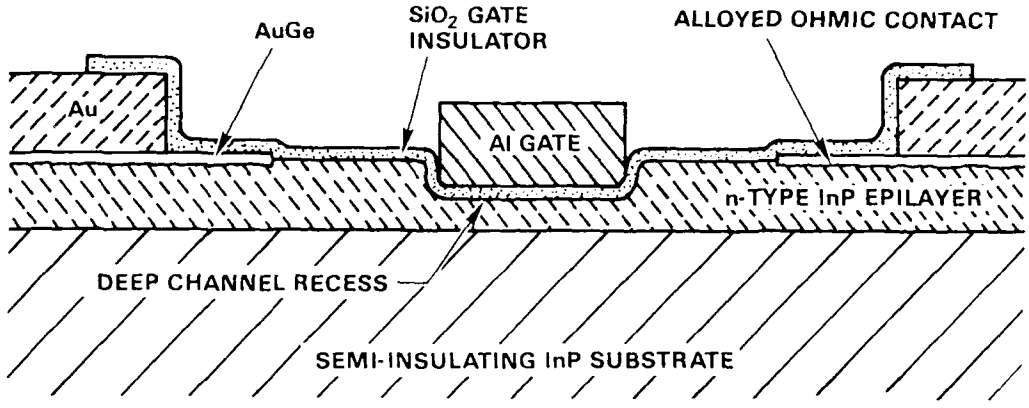


Figure 1. Mesa-type epitaxial InP power MISFET schematic cross-section.

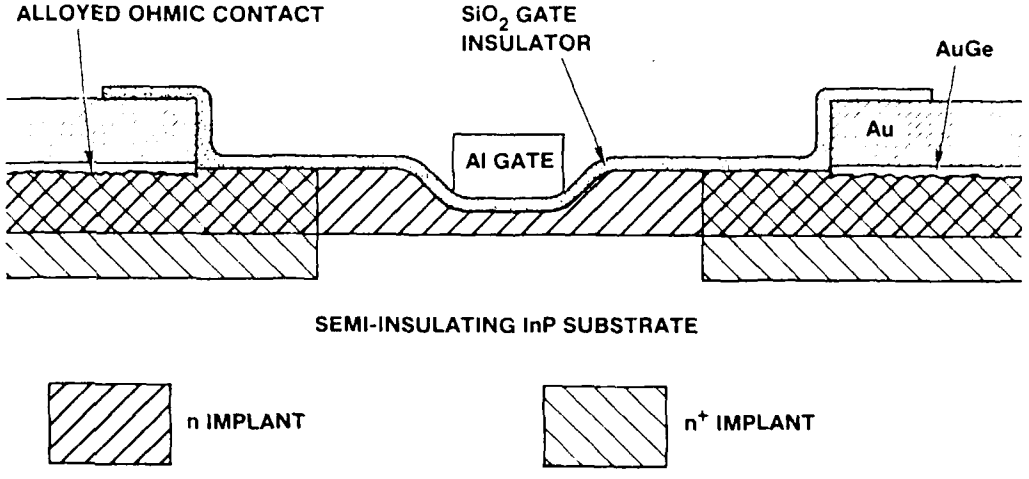
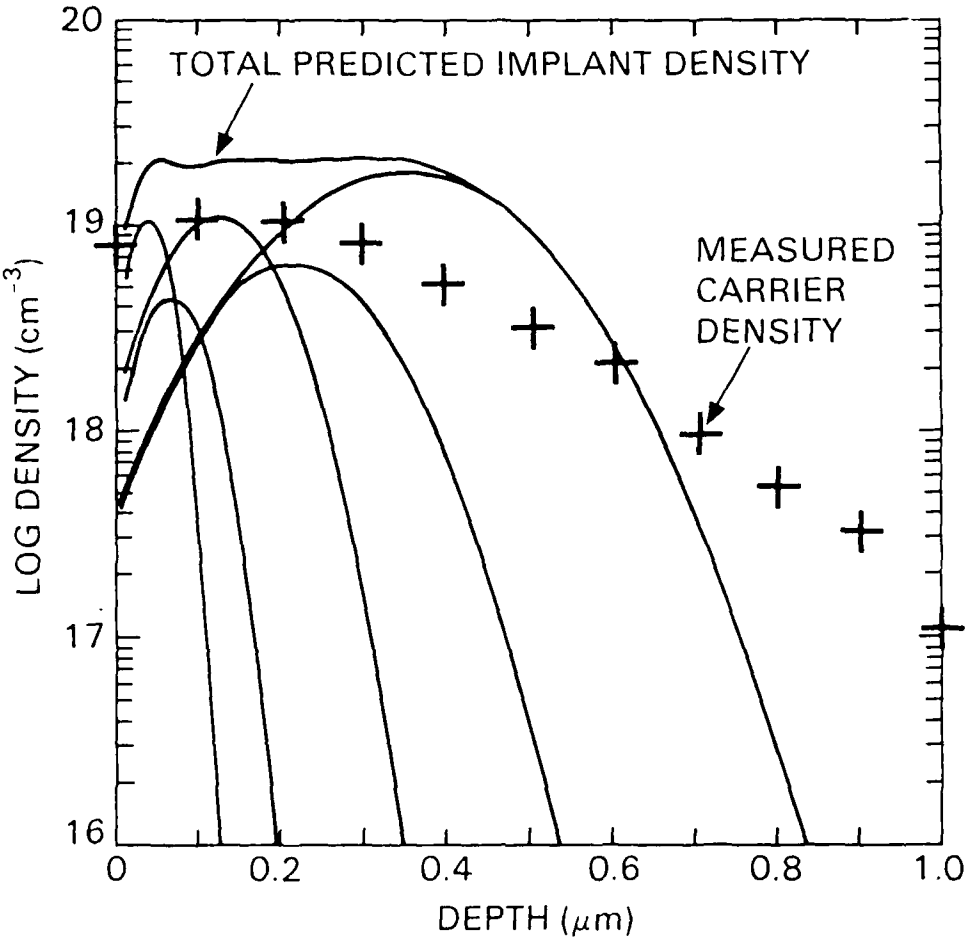
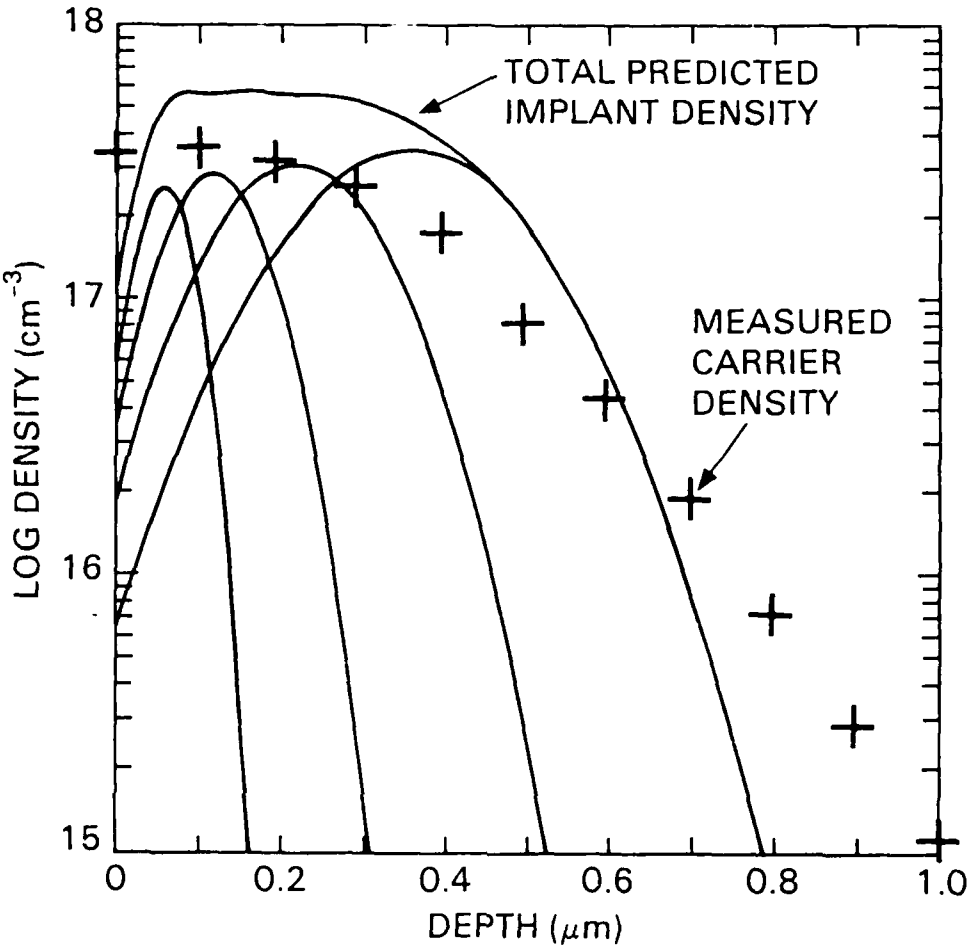


Figure 2. Planar fully ion-implanted InP power MISFET schematic cross-section.



Energy (KeV)	Dose(cm^{-2})	Range(μm)	Std. Dev.(μm)
360	5.6E14	0.355	0.126
220	1.4E14	0.215	0.091
130	1.7E14	0.125	0.061
70	3.9E13	0.067	0.037
40	6.0E13	0.038	0.024

Figure 3. Contact n^+ Si implant data, predicted impurity density vs. depth for each individual implant, total predicted impurity density and carrier density measured on a test sample.



Energy(keV)	Dose(cm^{-2})	Range(μm)	Std. Dev.(μm)
360	1.1E13	0.355	0.126
220	7.0E12	0.215	0.091
120	4.0E12	0.115	0.057
60	2.0E12	0.056	0.032

Figure 4. Typical channel n-type Si implant data, predicted impurity densities vs. depth for each individual energy implant, total predicted impurity density and carrier density measured on test sample.

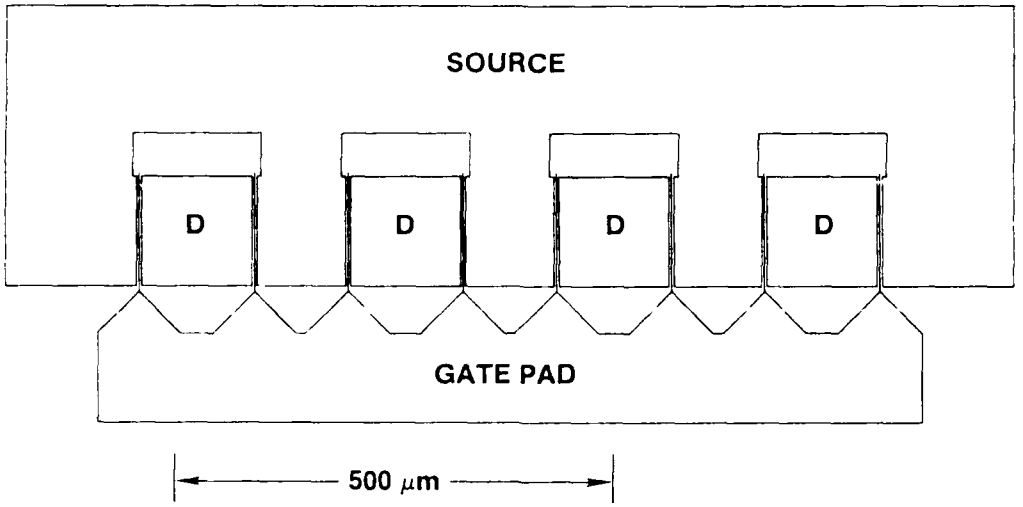


Figure 5. Epitaxial InP power MISFET geometry. For clarity only the contact n^+ implant and gate metallization regions are shown. Areas marked "D" are isolated drain regions requiring individual wire bonds. Implanted device geometries were basically the same.

	Implanted InP MISFET	Epitaxial InP MISFET	Best GaAs MESFET
Frequency	9.7 GHz	9.7 GHz	8 GHz
Gate Width	0.80 mm	1.0 mm	1.2 mm
V_{DS} (At Maximum Power Output)	16.3 V	18 V	18 V
V_{GS} (At Maximum Power Output)	-3.0 V	0 V	
I_{DS} (At Maximum Power Output)	269 mA	327 mA	152 mA
Power Output (4 dB Gain)	2.34 W*	4.5 W	1.7 W
Power-Added Efficiency	31%	46%	37%
I_{DS}/Gate Width	336 mA/mm	327 mA/mm	127 mA/mm
Power Output/Gate Width	2.9 W/mm	4.5 W/mm	1.4 W/mm

*3.7 dB Gain

Table III. CW power FET technology comparison.

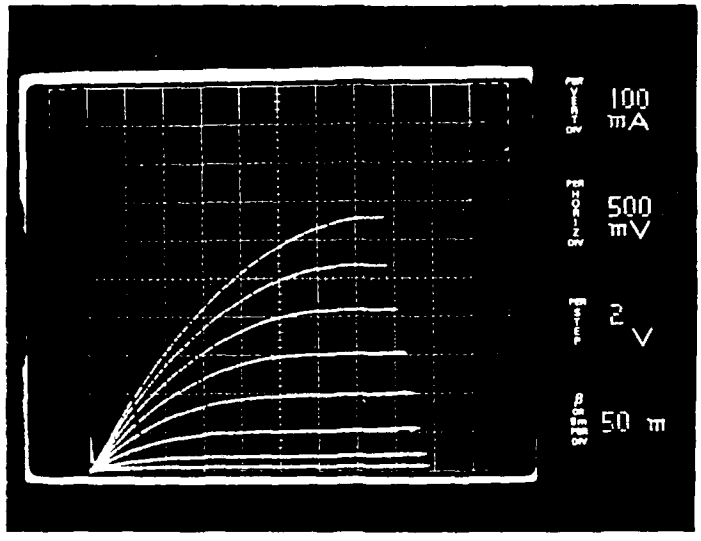


Figure 6. Drain characteristics of a representative 1 mm wide epitaxial InP depletion-mode power MISFET. 100 mA per major vertical division, 500 mV per major horizontal division, 2 V per step.

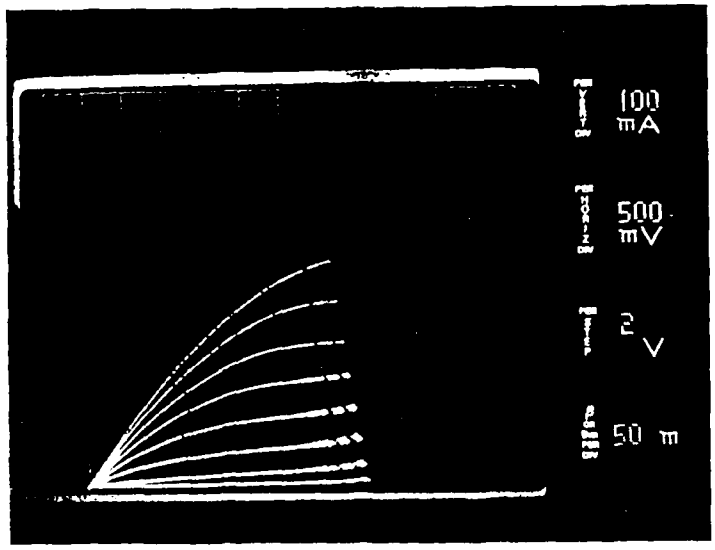


Figure 7. Drain characteristics of a representative 1 mm wide implanted InP depletion-mode power MISFET. 100 mA per major vertical division, 500 mV per major horizontal division, 2 V per step.

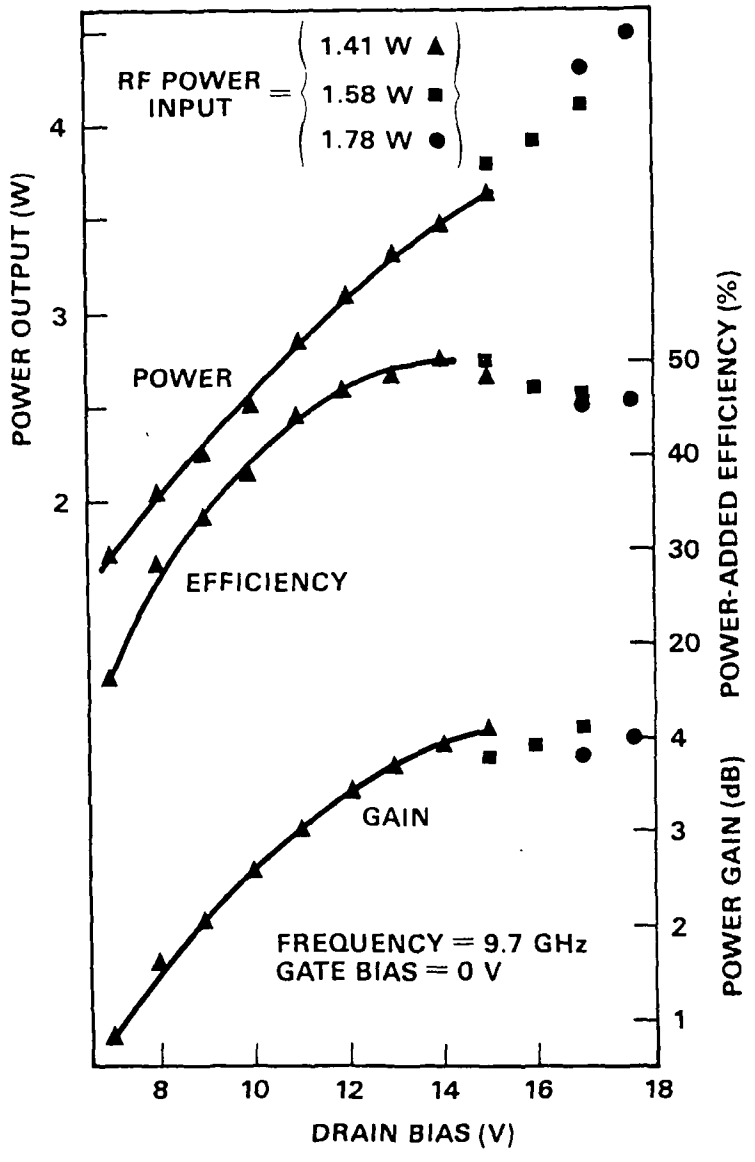


Figure 8. Dependence of power output, power-added efficiency and power gain on drain bias voltage and rf power input for a 1 mm gate width epitaxial InP MISFET. Implanted devices exhibited similar behavior.

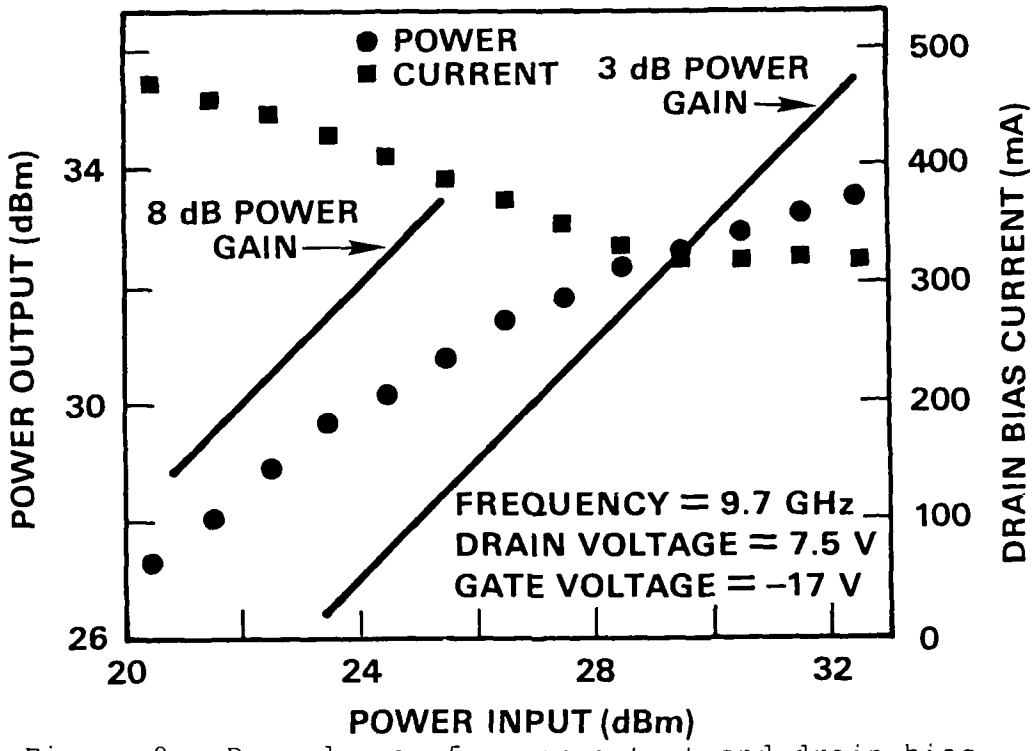


Figure 9. Dependence of power output and drain bias current on rf power input for a representative epitaxial InP MISFET.

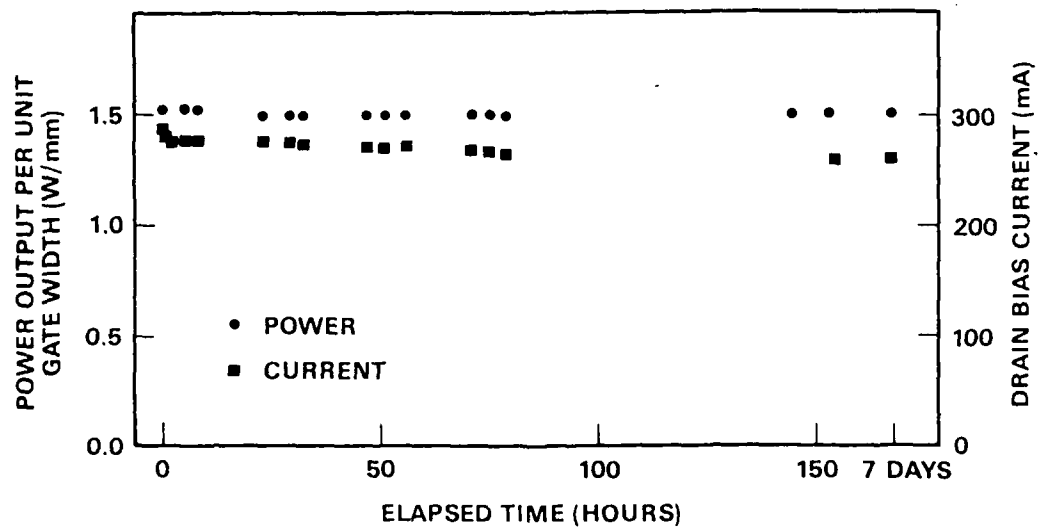


Figure 10. Time dependence of the power output and drain bias current of a representative 750 m wide epitaxial InP power MISFET with V_{DS}=9.5 V, V_{GS}=-7.5 V and an input rf power of 0.75 W/mm, all held constant, elapsed time equalling zero when these were first applied.

SUMMARY OF RESULTS

POWER OUTPUT 4.5 W AT 9.7 GHz CW WITH 4 dB GAIN

POWER DENSITY 4.5 WATTS PER MILLIMETER (OVER 3 TIMES THE HIGHEST GaAs VALUE)

POWER-ADDED EFFICIENCY AS HIGH AS 50%

POWER OUTPUT STABLE TO WITHIN 2% OVER 167 HOURS OF CONTINUOUS OPERATION

Table IV. Summary of the best InP power MISFET results, which are for the epitaxial devices.

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